

Notice of References Cited	Application/Control No. 09/976,395		Applicant(s)/Patent Under Reexamination LESEA ET AL.	
	Examiner Mark Connolly		Art Unit 2115	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,184,059	02-1993	Patino et al.	320/125
*	B	US-5,637,413	06-1997	Fernandez et al.	429/7
*	C	US-5,666,006	09-1997	Townsley et al.	307/66
*	D	US-5,698,971	12-1997	Sahai et al.	323/282
*	E	US-5,751,134	05-1998	Hoerner et al.	320/124
*	F	US-6,157,167	12-2000	Schwartz et al.	320/122
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	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Nelson et al, Digital Logic Circuit Analysis and Design, 1995, Prentice-Hall Inc., pgs 268-269.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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